CLAIMS:

1. A microprocessor control apparatus for uniformly reducing processor power independent of the processor logic, comprising:

a full power state machine control input;

a nap state machine control input;

a state machine ramp control;

a delay counter;

a pulse train generator;

a multiplexer;

a timed clock distribution control network;

a local clock buffer;

a full power state machine control input controlling the 'ramp down' request;

a nap state machine control input controlling the 'not ramp down' request input;

a full power state machine control input and a nap state machine control input coupled to a state machine ramp control;

a state machine ramp control connected to a delay counter and coupled to a pulse train generator;

a pulse train generator supplying and mixing pulses through a multiplexer connected to a timed clock control distribution network; and

a timed clock control distribution network coupled to a local clock buffer.

2. The system of claim 1, wherein the nap interrupt device is coupled to the state machine ramp control through the ramp down request module.

3. The system of claim 1, where a pulse train generator further comprises a delay counter unit and a state machine ramp control unit, wherein the pulse train generator is employed to transmit the pulse train to the timed clock control signal distribution network.

4. The system of claim 1, further comprising a local clock buffer control device employed to exercise control of the processor by means of conditioning the clock signal.

5. The system of claim 1, wherein the pulse trains from the pulse train generator drive the local clock buffer devices.

6. The system of claim 1, further comprising an external power analysis, wherein processor clocking power is analyzed for power requirements for all processor processes.

7. The system of claim 3, wherein the ramp down request device includes a signal device between the processor and the state machine ramp control to transmit the 'go to nap' command.

8. The system of claim 3, wherein the counter to create delay for next step unit includes an input/output loop to transmit signals to the state machine control ramp during a time period when the ramp down request is active.

9. The system of claim 4, wherein a local clock buffer device conditions a latch at a processor node.

10. The system of claim 3, wherein one or more devices can include a programmable memory storage device or input device.

11. A method for performing a plurality of shifts in clock frequency, comprising:

initiating a ramp down request as a function of a change in a power interrupt request;

incrementing a counter to start a state machine ramp control;

initiating a state machine ramp control logic;

selecting a pulse train from a pulse train generator;

masking a clocking power signal;

fanning out a pulse train;

driving a pulse train to the local clock buffers;

substantially halting a processor with a constant low signal; and

substantially restarting a processor at full power with a constant high signal.

12. The method of claim 11, wherein a pulse train is selected by a specific state within a state machine control ramp.

13. The method of claim 11, wherein a selected pulse train is multiplexing and masking a clocking power signal.

14. The method of claim 11, wherein a timed clock control distribution network is fanning out a pulse train.

15. The method of claim 11, wherein the multiplexed pulse train is driving local clock buffers.

16. The method of claim 11, wherein the local clock buffer is conditioning the pulse trains arriving through the timed clock control distribution network.

17. The method of claim 11, wherein the conditioned pulse train is latching processor gates.

18. The method of claim 11, wherein a zero pulse train effectively halts processor operation.

19. The method of claim 11, wherein a one pulse train is effectively sending full clocking power to the processor.

20. A computer program product for authenticating code in a computer system, the computer program product having a medium with a computer program embodied thereon, the computer program comprising:

computer code for accepting 'not ramp down' requests from less than full power modes;

computer code for accepting 'ramp down' requests from full power modes;

computer code for initiating a ramp down request as a function of a change in power interrupt request;

computer code for incrementing a counter to create a delay for initiating a state machine ramp control for a pulse train;

computer code for initiating a 'pass' or 'not passed' delay between state machine ramp control states;

computer code for selecting the appropriate pulse train; and

computer code for sending the selected pulse train to the local clock buffers.

21. A computer program for providing clocking power control in a computer system, the processor including a computer program comprising:

computer code for accepting 'not ramp down' requests from less than full power modes;

computer code for accepting 'ramp down' requests from full power modes;

computer code for initiating a ramp down request as a function of a change in power interrupt request;

computer code for incrementing a counter to create a delay for initiating a state machine ramp control for a pulse train;

computer code for initiating a 'pass' or 'not passed' delay between state machine ramp control states;

computer code for selecting the appropriate pulse train; and

computer code for sending the selected pulse train to the local clock buffers.